REMARKS

The Office Action dated January 5, 2010 has been received and considered. In this response, claim 36 has been amended and claim 79 has been added. Claim 47 has been cancelled without prejudice or disclaimer. Support for the amendments may be found in the specification and drawings as originally filed. For example, support for the amendment to claim 36 can be found at least at FIG. 1 of the application as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Anticipation Rejection of Claims 36-47 and 71-78 (McGuiness)

At page 3 of the Office Action, claims 36-47 and 71-78 are rejected under 35 U.S.C. § 102(e) as being anticipated by McGuinness et al. (US 2004/0078768). Claim 36 as amended recites "during compaction of a circuit layout, determining at a computer device a first direction associated with the circuit layout." Thus, claim 36 provides that the first direction is selected during compaction of a circuit layout. According to the Office Action at page 4, McGuiness discloses determining a first direction associated with a circuit layout at paragraphs 47 and 48. However, the cited paragraphs disclose only that a **cell layout** for a single transistor can be adjusted in order to fit the cell boundaries. The cited paragraphs do not refer to determining a first direction **during compaction of a circuit layout** in any manner. In particular, one skilled in the art understands that layout compaction is a procedure that occurs after circuit cells have been placed and routed into a circuit layout. This understanding is confirmed by FIG. 2 of McGuiness, which illustrates that a transistor of a cell is first folded (block 32 and FIG. 3) prior to placement of the transistor cells (block 36) and placement of cells representing other objects (block 38). After placement of the cells and routing (block 40), the resulting circuit layout is then compacted (block 42; *see also McGuiness* para. 26). Thus, McGuiness itself distinguishes between folding of a **transistor cell** and **compaction of a circuit layout**. Further, McGuiness discloses that the folding of the transistor cell cited by the Office as disclosing the features of claim 36 occurs prior to compaction of the circuit layout. *Id.*, FIG. 2 and FIG. 4.

In addition, claim 36 has been amended to recite ""determining at the computer device a second direction associated with the circuit layout, the second direction different from the first direction; …[and] in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the second direction." Thus, claim 36 provides for adjusting the size of a first logical device in a first direction and a second logical device **in a different direction** than the first direction. The Office Action asserts at page 4 that these features are discloses at paragraphs 47 and 48 of McGuiness. However, the cited paragraphs disclose only that finger sizes on the left and right of a cell can be adjusted to fit within a target cell height. Thus, paragraphs 47 and 48 disclose adjusting the size of a cell **in a single direction**. Even assuming *arguendo* that adjusting the size of a cell corresponds to compaction of a circuit layout, there is no disclosure that the layout of the cell is reduced **in two different directions** as provided by claim 36. Thus, McGuiness fails to disclose at least the above-cited features of claim 36.

Claims 37-46 and 71-78 depend from claim 36. Accordingly, McGuiness fails to disclose at least one feature of each of these dependent claims, at least by virtue of their dependence on claim 36. In addition, these claims recite additional novel features.

Claim 47 has been cancelled without prejudice or disclaimer, thereby obviating its rejection.

In view of the foregoing, withdrawal of the above-referenced anticipation rejection and reconsideration of the claims is respectfully requested.

Anticipation Rejection of Claims 36-47 and 71-78 (Gupta)

At page 3 of the Office Action, claims 36-47 and 71-78 are rejected under 35 U.S.C. § 102(b) as being anticipated by Gupta (US 6,163,877). This rejection is hereby respectfully traversed.

Claims 36 recites "**during compaction of a circuit layout**, determining at a computer device a first direction associated with the circuit layout; [and] selecting at the computer device a first portion of a first transistor in response to determining the first portion extends outward in the first direction from a first logical device of the circuit layout, the first logical device

comprising the first transistor." According to the Office Action at page 4, Gupta discloses these features at column 7, lines 33-40. However, the cited portion discloses only that transistors in a cell exceeding a specified height can be folded to reduce the height of the cell. As a first issue, there is no disclosure that the transistors are folded **during a compaction of a circuit layout**, as provided by claim 36. Instead, FIG. 9 of Gupta discloses that the transistor folding is performed at block 906 prior to determining a layout at block 922.

Further, claim 36 provides that a first portion of the transistor is selected **in response to determining the first portion extends outward in the first direction from a first logical device of the circuit layout, the first logical device comprising the first transistor**. Gupta nowhere discloses that the portion of the transistors that are folded are selected based on those portions extending outward in a first direction from a logical device in any manner. In other words, claim 36 provides that the portion of a transistor that is reshaped is selected based on its extension from a logical device in a first direction. Gupta discloses that a transistor can be folded based on the transistor cell exceeding a specified height. Assuming *arguendo* that the transistor of Gupta is part of a logical device, there is no disclosure by Gupta that any portion of the transistor is selected for folding based on the portion extending outward from the logical device in a selected direction. In particular, there is no disclosure by Gupta that the cell height of the transistor cell is oriented in such a way that the transistor extends outward from a logical device in any manner. Accordingly, Gupta fails to disclose at least the above-cited features of claim 36.

In addition, claim 36 as amended recites ""determining at the computer device a second direction associated with the circuit layout, the second direction different from the first direction; …[and] in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the second direction." Thus, claim 36 provides for adjusting the size of a first logical in a first direction and a second logical device **in a different direction** than the first direction. The Office Action asserts at page 4 that these features are discloses at paragraphs column 7, lines 33-40 of Gupta. However, the cited paragraphs disclose only that a transistor of a transistor cell can be folded to fit within a target cell height. Thus, Gupta discloses adjusting the size of a cell **in a single direction**. Even assuming *arguendo* that adjusting the size of a cell corresponds to compaction

of a circuit layout, there is no disclosure that the layout of the cell is reduced **in two different directions** as provided by claim 36. Thus, Gupta fails to disclose at least the above-cited features of claim 36.

Claims 37-46 and 71-78 depend from claim 36. Accordingly, McGuiness fails to disclose at least one feature of each of these dependent claims, at least by virtue of their dependence on claim 36. In addition, these claims recite additional novel features.

Claim 47 has been cancelled without prejudice or disclaimer, thereby obviating its rejection.

In view of the foregoing, withdrawal of the above-referenced anticipation rejection and reconsideration of the claims is respectfully requested.

New Claim

Claim 79 has been added, and recites features not disclosed by the cited references. For example, claim 79 recites "during compaction of a circuit layout, determining at a computer device a first direction associated with the circuit layout." As explained above, neither of the cited references discloses compaction of a circuit layout. Therefore, the cited references fail to disclose at least the above-cited features of claim 79. Consideration and allowance of claim 79 is respectfully requested.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-3797.

Respectfully submitted,

/Adam D. Sheehan/ April 5, 2010

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